SFP, 1.25Gbps, LC, 3.3V, sm, 1310nm, DDM, 0-20km

Особенности:
- возможность горячей замены
- двойной LC разъем
- детальная информация о модули в EEPROM
- Digital diagnostic monitor interface (DDMI)
- соответствие спецификации SFP MSA и SFF-8472

Области применения:
- Gigabit Ethernet 1000Base-LX
- ATM
- SONT/SDH/PDH
- FDDI
- Fiber Channel

Absolute maximum ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	+85	℃
Operating Temperature	T_{op}	-5	+70	℃
Supply Voltage	V_{CC}	-0.5	+4.0	V
Voltage at any Input Pin	V_{IN}	0	Vcc	V
Power supply current	I_{CC}	-	300	mA

Operating Conditions

Transmitter（T=0 to +70℃, V_{CC} =3.1~3.5V)

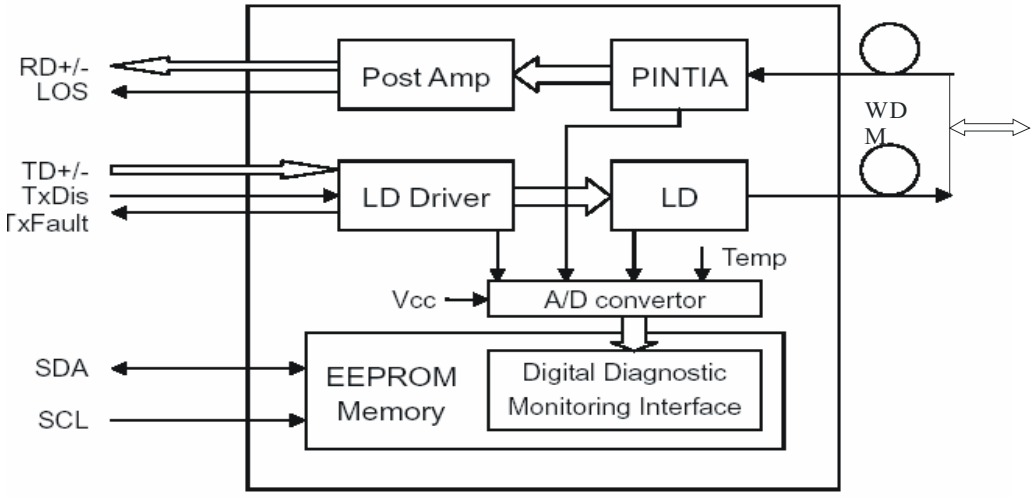
Parameter	Symbol	Min.	Typ.	Max.	Unit
Central Wavelength	λ_C	1270	1310	1350	nm
Spectral Width	$\Delta\lambda$	-	-	3	nm
Output Power	P_o	-8	-	-3	dBm
Extinction Ratio	ER	9	-	-	dB
Optical Rise/Fall Time	T_r / T_f	-	-	260	ps
Total Jitter	TJ	-	-	227	ps
P_{OUT} @TX Disable Asserted	P_{off}	-	-	-45	dBm
Differential Input Voltage	V_{DIFF}	500	-	2400	mV
Transmit Fault Output-Low	TX_FAULTL	0	-	0.8	V
Transmit Fault Output-High	TX_FAULTH	2.0	-	V_{CC}	V
TX_DISABLE Assert Time	$t_{\_off}$	-	-	10	μs
TX_DISABLE Negate Time	$t_{\_on}$	-	-	1	ms

Time to Initialize, Include Reset of TX_FAULT	t_{init}	-	-	300	ms
TX_FAULT From Fault to Assertion	t_{fault}	-	-	100	μs
TX_DISABLE Time to Start Reset	t_{reset}	10	-	-	μs

Receiver （T=0 to +70℃, Vcc=3.1~3.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Wavelength Range	λ	1270	-	1620	nm
MIN. Input Power (Sensitivity)	P_{MIN}	-	-	-21	dBm
MAX. Input Power (Saturation)	P_{MAX}	-3	-	-	dBm
Signal Detect-Asserted	P_A	-	-	-21	dBm
Signal Detect-De-Asserted	P_D	-35	-	-	dBm
Signal Detect Hysteresis	P_{HYS}	0.5	-	5	dB
Receiver Loss of Signal Output Voltage-Low	RX_LOSL	0	-	0.8	V
Receiver Loss of Signal Output Voltage-High	RX_LOSH	2.0	-	V_{CC}	V
LOS Assert Time	t_{loss_on}	-	-	100	μs
LOS De-Assert Time	t_{loss_off}	-	-	100	μs

Block Diagram of Transceiver



EEPROM Description

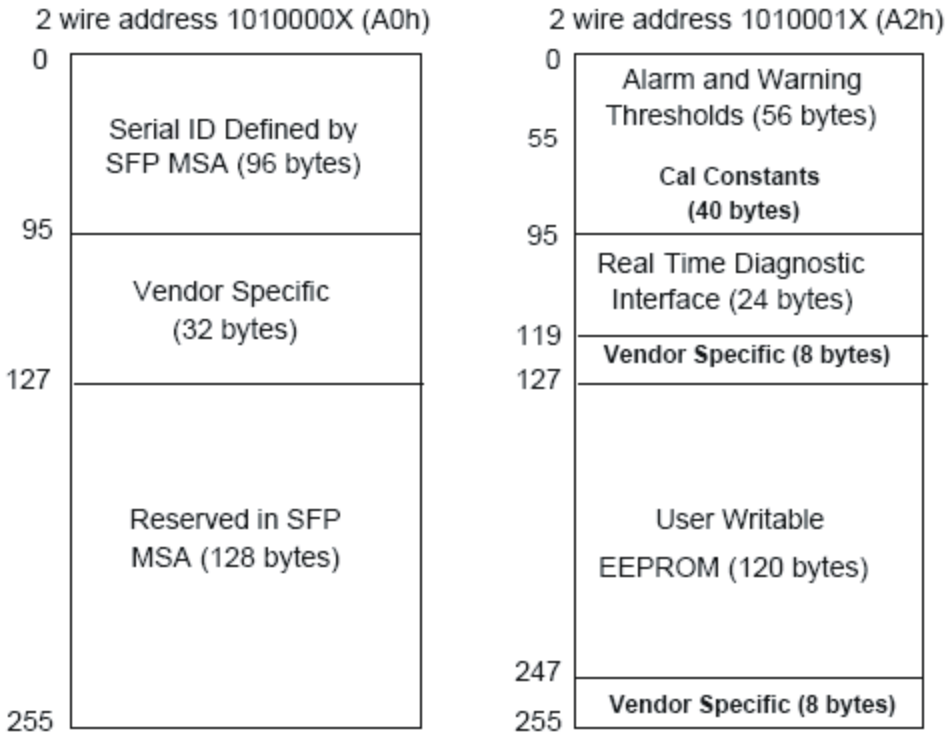
The SFP serial ID provides access to sophisticated identification information that describes the transceiver's capabilities, standard interfaces, manufacturer, and other information. The serial

interface uses the 2-wire serial CMOS E2PROM protocol defined for the ATMEL AT24C01A/02/04 family of components.
When the serial protocol is activated, the host generates the serial clock signal (SCL, Mod Def 1). The positive edge clocks data into those segments of the E2PROM that are not write-protected within the SFP transceiver. The negative edge clocks data from the SFP transceiver.
The serial data signal (SDA, Mod Def 2) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

Monitoring Interface

The interface is an extension of the serial ID interface defined in the SFP MSA specification. The specifications define a 256 byte memory map in EEPROM which is accessible over a 2 wire serial interface at the 8 bit address 1010000X (A0h). The digital diagnostic monitoring interface makes use of the 8 bit address 1010001X (A2h), so the originally defined serial ID memory map remains unchanged. The interface is backward compatible with both the GBIC specification and the SFP MSA. Please see Figure 1.

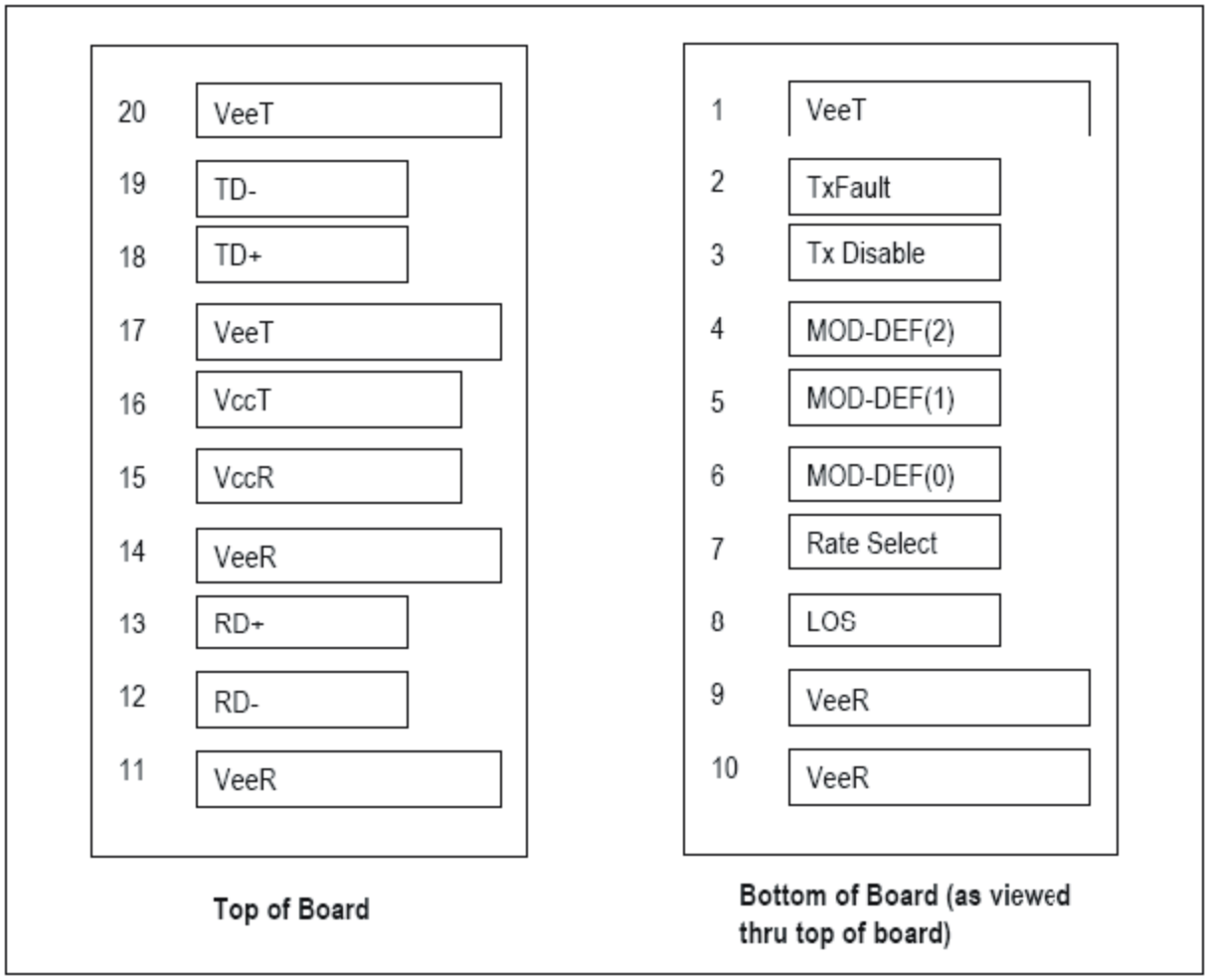
Figure 1, Digital Diagnostic Memory Map Specific Data Field Descriptions



Pin Assignment and Function Definitions

It is the responsibility of the system integrator to assure that no thermal, energy, or voltage hazard exists during the hot-plug-unplug sequence. It is also the responsibility of the system integrator and end-user to minimize static electricity and the probability of ESD events by careful design.

Pins Assignment

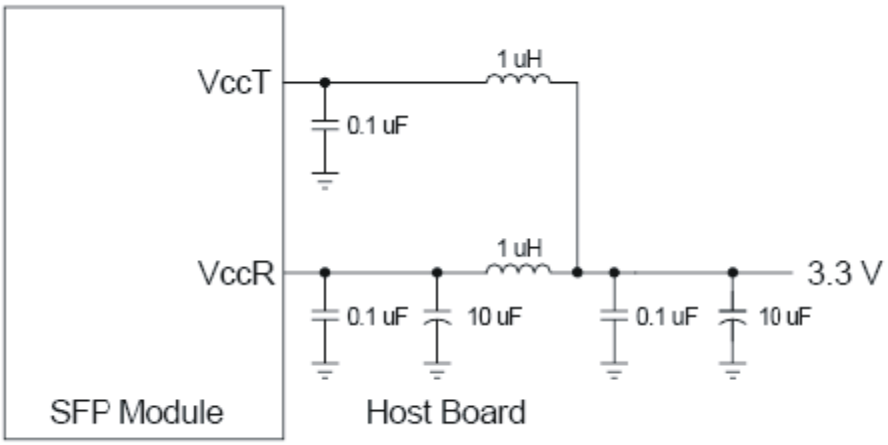


Pin No.	Name	Function	Plug Seq.	Notes
	Function definition			
1	VeeT	Transmitter Ground	1	
2	TX Fault	Transmitter Fault Indication	3	Note 1
3	TX Disable	Transmitter Disable	3	Note 2
4	MOD-DEF2	Module Definition 2	3	Note 3
5	MOD-DEF1	Module Definition 1	3	Note 3
6	MOD-DEF0	Module Definition 0	3	Note 3
7	Rate Select	Not Connected	3	

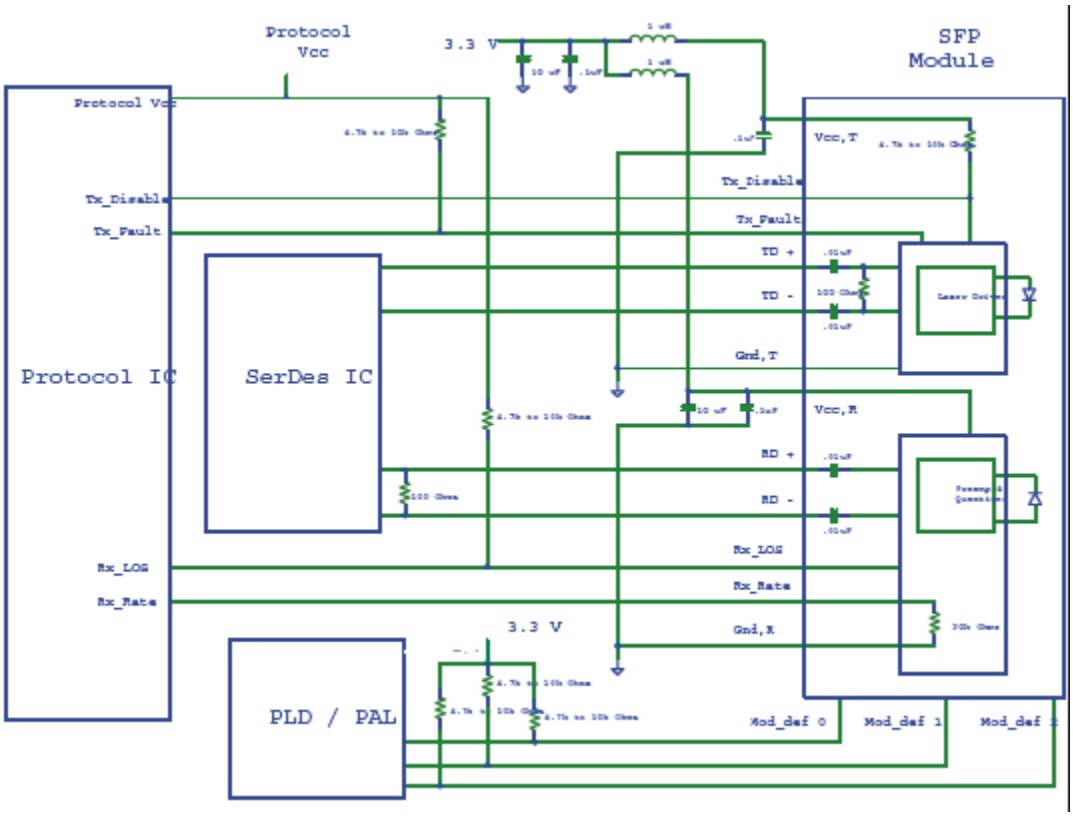
8	LOS	Loss of Signal	3	Note 4
9	VeeR	Receiver Ground	1	
10	VeeR	Receiver Ground	1	
11	VeeR	Receiver Ground	1	
12	RD-	Inv. Received Data Out	3	Note 5
13	RD+	Received Data Out	3	Note 5
14	VeeR	Receiver Ground	1	
15	VccR	Receiver Power	2	
16	VccT	Transmitter Power	2	
17	VeeT	Transmitter Ground	1	
18	TD+	Transmit Data In	3	Note 6
19	TD-	Inv Transmit Data In	3	Note 6
20	VeeT	Transmitter Ground	1	

Notes:
1. TX Fault is an open collector output, which should be pulled up with a 4.7K~10K. resistor on the host board to a voltage between 2.0V and Vcc+0.3V. Logic 0 indicates normal operation; logic 1 indicates a laser fault of some kind. In the low state, the output will be pulled to less than 0.8V.
2. TX Disable is an input that is used to shut down the transmitter optical output. It is pulled up within the module with a 4.7K~10K resistor. Its states are:
Low (0~0.8V): Transmitter on
(>0.8V, <2.0V): Undefined
High (2.0~3.465V): Transmitter Disabled
Open: Transmitter Disabled.
3. MOD-DEF 0,1,2 are the module definition pins. They should be pulled up with a 4.7K~10K resistor on the host board. The pull-up voltage shall be VccT or VccR.
MOD-DEF 0 is grounded by the module to indicate that the module is present.
MOD-DEF 1 is the clock line of two wire serial interface for serial ID.
MOD-DEF 2 is the data line of two wire serial interface for serial ID.
4. LOS is an open collector output, which should be pulled up with a 4.7K~10K resistor on the host board to a voltage between 2.0V and Vcc+0.3V. Logic 0 indicates normal operation; logic 1 indicates loss of signal. In the low state, the output will be pulled to less than 0.8V.
5. These are the differential receiver outputs. They are AC coupled 100.differential lines which should be terminated with 100. (differential) at the user SERDES.
6. These are the differential transmitter inputs. They are AC-coupled, differential lines with 100.differential termination inside the module.

 Recommended Host Board Supply Filtering Network



Example SFP Host Board Schematic SFP


Protocol
Vcc
3.3 V
SFP
Module
Protocol Vcc
Tx_Disable
Tx_Fault
Protocol IC
SerDes IC
Rx_LOS
Rx_Rate
PLD / PAL
3.3 V
Vcc,T
Tx_Disable
Tx_Fault
TD +
TD -
Gnd,T
Vcc,R
RD +
RD -
Rx_LOS
Rx_Rate
Gnd,R
Mod_def 0
Mod_def 1
Mod_def 2